ABSTRACT

FACILITATING INTER-DSP DATA COMMUNICATIONS

A method, computer program product and system for facilitating inter-digital signal processing (DSP) data communications. A direct memory access (DMA) controller may be configured to facilitate transfers of data between a first and a second DSP processor core coupled to the DMA controller. The DMA controller may read a data structure, referred to as a "buffer descriptor block," to perform the data transfer. The buffer descriptor block may store both a source address and a destination address indicating where the data is to be retrieved and stored. The buffer descriptor block may further store a value, e.g., number of bytes, indicating a size of the data to be transferred. The DMA controller may then transfer the data located at the source address in the first DSP processor core, with a size, e.g., number of bytes, indicated from the buffer descriptor block, to the destination address in the second DSP processor core.